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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/816,099	03/26/2001	Tomohisa Kimura	205129US2RD	8874

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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
SHAAWAT, MUSSA	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,099	KIMURA ET AL.	
	Examiner	Art Unit	
	Mussa A Shaawat	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *26 March 2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to application # 09/816,099, filed on March 26, 2001. Claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated *by "Stable and Efficient Reduction of Substrates Model Networks Using Congruence Transforms"*, Kevin J. Kerns, Ivan L. Wemple, and Andrew T. Yang, ICCAD95_0207 referred to hereinafter as Kerns.

As to claim 1, KERNS teaches a semiconductor device analyzer (see Page 3, 2nd paragraph, the device being a program running on a computer which in this case corresponds to the commercially available SPICE program running on a computer) comprising:

A substrate model-reading module configured to read, from input data to the semiconductor device analyzer (see page 4 col.1 paragraph 2, where the device is a program running on a computer in this case the device is the commercially available SPICE program from which the substrate model input data is read),

A substrate network model of three-dimensional meshes representing a substrate of a semiconductor device at a surface (see page 1 col.1 Introduction section 2nd paragraph lines 5-9) of and in which circuit elements are merged (see page 1 Introduction section 3rd paragraph lines 7-11 where eliminating the internal nodes leads to network reduction which corresponds elements of a circuit being merged);

A Y-matrix entry module configured to prepare a Y-matrix from the substrate network model and express each element of the Y-matrix with a polynomial of differential operator "s" (see page 4, col.1 paragraph 1 and 2, note in the specification on page 1 paragraph [0008] the applicant equates the Y-matrix to be called the admittance matrix, Kerns uses commercially available SPICE program to prepare an admittance matrix which in this case corresponds to Y-Matrix, the differential operator "s" defined in page 6 paragraph [0074] of the specification to be the complex angular frequency);

A discriminating module configured to discriminate internal nodes to be eliminated from and external nodes to be left in the substrate network model (see Page 1, col.2 paragraph 2 and col.2 paragraph 1, Kerns uses commercially available SPICE program that includes a module to eliminate the internal nodes of the substrate network model);

And a matrix reduction module configured to reduce the Y-matrix by eliminating the internal nodes (see page 1 col.2 paragraph 2, Page 6 col.2 paragraph 1, Kerns uses commercially available SPICE program that includes a matrix reduction module to eliminate the internal nodes of the substrate network model).

As to claim 2, KERNS teaches an analyzer of claim 1, further comprising an input unit configured to set an upper limit on the degree of the polynomial of differential operator "s" (see page 4, col.1 paragraph 1 and 2, Kerns uses commercially available SPICE program to prepare an admittance matrix which in this case corresponds to Y-Matrix, the complex frequency "s" taught by Kerns corresponds to the differential operator "s", network poles are retained from DC to a specified upper frequency limit which corresponds to setting an upper limit on the degree of polynomial of differential operator "s").

As to claim 3, KERNS teaches an analyzer of claim 1, further comprising an output format-determining module configured to determine an output format for an operation result provided by the matrix reduction module (see page 4 col.1 paragraph 2, Page 6 col.2 paragraph 1, Kerns uses commercially available SPICE program that comprises a module to determine an output format of the reduced format).

As to claim 4, KERNS teaches a method for analyzing semiconductor device (see Page 3, 2nd paragraph, the device being a program running on a computer which in this case corresponds to the commercially available SPICE program running on a computer), comprising:

Discriminating, among data prescribed in an input format for a circuit simulator, data expressing a substrate network model of three-dimensional meshes representing a substrate of the semiconductor device at a surface (see page 1 col.1 Introduction section 2nd paragraph lines 5-9) of and in which circuit elements are merged (see page 1 Introduction section 3rd paragraph lines 7-11 where eliminating the internal nodes leads to network reduction which corresponds elements of a circuit being merged);

Reading the data expressing the substrate network model (see page 4 col.1 paragraph 2, where the device is a program running on a computer in this case the device is the commercially available SPICE program from which the substrate model input data is read);

Preparing a Y-matrix from the data expressing the substrate network model; expressing each element of the Y-matrix with a polynomial of differential operator "s" (see page 4, col.1 paragraph 1 and 2, note in the specification on page 1 paragraph [0008] the applicant equates the Y-matrix to be called the admittance matrix, Kerns uses commercially available SPICE program to prepare an admittance matrix which in this case corresponds to Y-Matrix, the differential

operator "s" defined in page 6 paragraph [0074] of the specification to be the complex angular frequency);

Discriminating elements of the Y-matrix corresponding to internal nodes to be eliminated from and external nodes to be left in the substrate network model (see Page 1, col.2 paragraph 2 and col.2 paragraph 1, Kerns uses commercially available SPICE program that includes a module to eliminate the internal nodes of the substrate network model); and

Reducing the Y-matrix by eliminating the internal nodes (see page 1 col.2 paragraph 2, Page 6 col.2 paragraph 1, Kerns uses commercially available SPICE program that includes a matrix reduction module to eliminate the internal nodes of the substrate network model).

As to claim 5, KERNS teaches a method of claim 4, further comprising externally setting an upper limit on the degree of the polynomial of differential operator "s" (see page 4, col.1 paragraph 1 and 2, Kerns uses commercially available SPICE program to prepare an admittance matrix which in this case corresponds to Y-Matrix, the complex frequency "s" taught by Kerns corresponds to the differential operator "s", network poles are retained from DC to a specified upper frequency limit which corresponds to setting an upper limit on the degree of polynomial of differential operator "s").

As to claim 6, KERNS teaches a method of claim 4, further comprising determining whether or not the dimension of the reduced Y-matrix is equal to the number of the external nodes and iterating, until the dimension of the reduced Y-matrix becomes equal to the number of the external nodes, a sequence including the reading step, Y-matrix preparing step, polynomial expressing step, discriminating step, and Y-matrix reducing step (see Page 4 col.1 paragraph 2, Page 2 col.1 paragraph 3, and Page 3 col.1 paragraph 3, the method used by Kerns to reduce the

Y-matrix includes the sequence of a reading step, preparing step polynomial expressing step, discriminating step and Y-matrix reducing step).

As to claim 7, KERNS teaches a method of claim 4, further comprising leaving the reduced Y-matrix whose dimension is equal to the number of the external nodes as it is so as to provide stamps (see Page 4 col.1 paragraph 2, where the reduced matrix is stamped to be easily realized by the reduced RC network in a SPICE-compatible net list format).

As to claim 8, KERNS teaches a method of claim 4, further comprising determining an output format for the reduced Y-matrix (see page 4 col.1 paragraph 2, Page 6 col.2 paragraph 1, Kerns uses commercially available SPICE program that comprises a module to determine an output format of the reduced format).

As to claim 9, KERNS teaches a method of claim 8, wherein the output format is one of a resistive network reconstituted from the reduced Y-matrix, an RC network reconstituted from the reduced Y-matrix, a circuit matrix based on the reduced Y-matrix and representing a multi-port network, and an RC or RCL network of filter circuits based on the reduced Y-matrix (see Page 4 col.1 section 3.1).

As to claim 10, KERNS teaches a method of claim 4, further comprising reconstituting data in the input format for the circuit simulator from the reduced Y-matrix (see Page 6 col.2 paragraph 1).

As to claim 11, KERNS teaches a method of claim 4, wherein the substrate network model is made of an RC network (see Page 1 col.1 paragraph 1).

As to claim 12, KERNS teaches a method for manufacturing a semiconductor device (see Page 3, 2nd paragraph, the device being a program running on a computer which in this

case corresponds to the commercially available SPICE program running on a computer) comprising:

Discriminating, among data prescribed in an input format for a circuit simulator, data expressing a substrate network model of three-dimensional meshes representing a substrate of the semiconductor device at a surface (see page 1 col.1 Introduction section 2nd paragraph lines 5-9) of and in which circuit elements are merged (see page 1 Introduction section 3rd paragraph lines 7-11 where eliminating the internal nodes leads to network reduction which corresponds elements of a circuit being merged);

Reading the data expressing the substrate network model (see page 4 col.1 paragraph 2, where the device is a program running on a computer in this case the device is the commercially available SPICE program from which the substrate model input data is read);

Preparing a Y-matrix from the data expressing the substrate network model; expressing each element of the Y-matrix with a polynomial of differential operator "s" (see page 4, col.1 paragraph 1 and 2, note in the specification on page 1 paragraph [0008] the applicant equates the Y-matrix to be called the admittance matrix, Kerns uses commercially available SPICE program to prepare an admittance matrix which in this case corresponds to Y-Matrix, the differential operator "s" defined in page 6 paragraph [0074] of the specification to be the complex angular frequency);

Discriminating elements of the Y-matrix corresponding to internal nodes to be eliminated from and external nodes to be left in the substrate network model (see Page 1, col.2 paragraph 2 and col.2 paragraph 1, Kerns uses commercially available SPICE program that includes a module to eliminate the internal nodes of the substrate network model); and

Reducing the Y-matrix by eliminating the internal nodes (see page 1 col.2 paragraph 2, Page 6 col.2 paragraph 1, Kerns uses commercially available SPICE program that includes a matrix reduction module to eliminate the internal nodes of the substrate network model);

Reconstituting data in the input format for the circuit simulator from the reduced Y-matrix (see page 3 col.1 section 3 paragraph 1, circuit simulation and timing analysis are easily realized by SPICE program); and carrying out a circuit simulation with the reconstituted data for the circuit simulator, to analyze the influence of parasitic elements in the substrate on wiring capacitance of the semiconductor device (see Page 2 section 1, last paragraph lines 21-29, where a method is used to form a unified, efficient strategy for developing parasitic substrate models for mixed-signal circuit simulation and design verification).

As to claim 13, KERNS teaches a method of claim 12, further comprising: carrying out a process simulation based on required design specifications, to provide doping profiles in the substrate; and carrying out a device simulation according to the doping profiles provided by the process simulation and given electric boundary conditions so that the data in the circuit simulator input format is provided as the output data of the device simulation (see page 6 col.2 paragraph 3).

As to claim 14, KERNS teaches a method of claim 13, wherein the device simulation provides device behavior of the semiconductor device as an input data for the circuit simulation (see Page 6 col.1 paragraph 2).

As to claim 15, KERNS teaches a method of claim 12, further comprising determining whether or not a result of the circuit simulation satisfies required circuit performances (see Page 6 col.1 paragraph 4).

As to claim 16, KERNS teaches a method of claim 15, further comprising designing, if the result of the circuit simulation satisfies the required circuit performances, mask patterns based on the data provided by the process simulation, device simulation, and circuit simulation and fabricating a set of masks (see Page 1 col.1 paragraph 3, Page 6 col.1 paragraph 4).

As to claim 17, KERNS teaches a method of claim 16, further comprising carrying out a wafer process with use of the set of masks (see Page 6 col.2 paragraph 3, Page 1 col.1 paragraph 3).

As to claim 18, the limitations of claim 18 are similar to the limitations of claim 1; therefore they are rejected based on the same rationale, supra.

As to claim 19, the limitations of claim 19 are similar to the limitations of claim 6; therefore they are rejected based on the same rationale, supra.

As to claim 20, the limitations of claim 20 are similar to the limitations of claim 7; therefore they are rejected based on the same rationale, supra.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Kumashiro US Patent No. (6,360,190) Semiconductor process device simulation method and storage medium storing simulation program.
- Milsom US Patent No. (6,031,986) Thin-Film circuit simulation on basis of reduced equivalent circuits.
- Yang et al., US Patent No. (5,469,366) Method and apparatus for determining the performance of nets of a semiconductor design automation system.

- Hiroi et al. US Patent No. (5,986,263) electron beam inspection method and apparatus and semiconductor manufacturing method and its manufacturing line utilizing the same.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mussa A Shaawat whose telephone number is (571) 272-3785. The examiner can normally be reached on Monday-Friday (8:30am to 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R Homere can be reached on (571) 272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mussa Shaawat
Patent Examiner
December 13, 2004

JEAN R. HOMERE
PRIMARY EXAMINER